Compact MOSFET modeling for sub-100nm CMOS circuit analysis

1. MOTIVATION

The accuracy and computational efficiency of CMOS circuit analysis models is directly affected by the accuracy and the simplicity of the used MOSFET model. Such a model must meet two equally important requirements:

- accurate transistor drain current prediction, and
- simplicity of the device model to obtain explicit expressions for design parameters (i.e. transient response, energy dissipation).

In most existing MOSFET I-V models, the effects that determine the device behavior are accounted for through physical and empirical parameters.

With the growing complexity of physical mechanisms in nanometer devices, MOSFET I-V models become very complex and employ a large number of parameters to provide the highest accuracy. Although these complex but accurate models can be handled by circuit simulators, they do not satisfy the requirement of computational efficiency.

Hence, compact MOSFET models are needed, as simple as possible to take into account the influences of essential physical mechanisms in nanometer devices by using few parameters extracted through measurements or simulations.

2. MAIN EFFECTS IN NANOMETER DEVICES

In order to support CMOS circuit modeling, an accurate and compact I-V model for nanometer MOSFETs is needed. The I-V equations of such model may use empirical parameters to match measured or simulated device characteristics.

The influence of predominant effects in nanometer devices should be taken into account:

- mobility degradation and velocity saturation,
- channel-length modulation,
- drain-induced barrier lowering (DIBL),
- body effect,
- narrow channel width,
- source-drain parasitic resistance.

3. MOBILITY DEGRADATION EFFECT

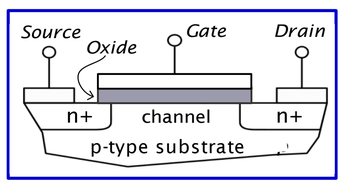
For small electric fields, the carriers' mobility is constant and independent of the applied electric field.

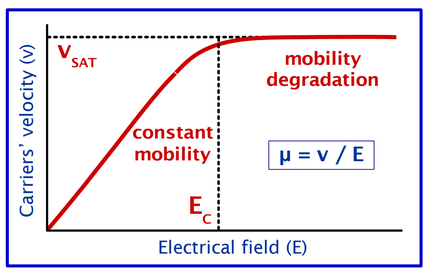
When the horizontal electrical field (moving the channel carriers) reaches a critical value, the carriers velocity tends to saturate due to scattering effect (i.e. electrons moving in semiconductor material collide with silicon atoms).

This effect is more pronounced for reduced channel length that implies higher horizontal electric fields for equivalent drain-source voltages.

The vertical electric field originating from the gate voltage further inhibits channel carrier mobility.

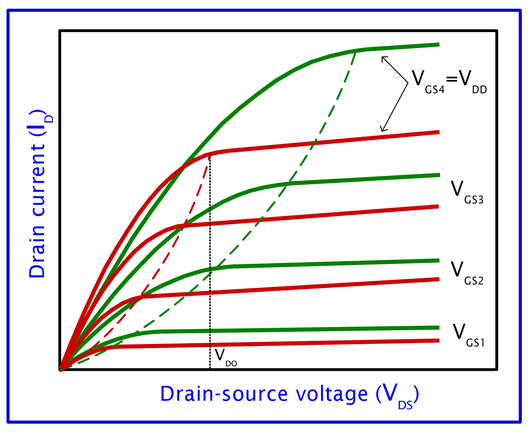
This field pushes carriers toward the gate oxide and the carriers' mobility is reduced due to carrier collisions with the oxide-channel interface.





Influence of the effect on the device output characteristics:

- saturation is achieved at smaller drain-source voltages,
- the spacing of the I-V curves in saturation is not according to square law, but becomes nearly proportional to gate-source voltage increment.



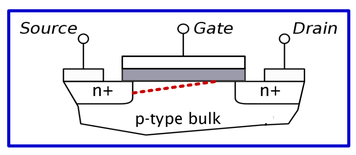
The modeling of mobility degradation and velocity saturation effects is achieved by employing the velocity saturation index (α) to describe the power laws featuring the drain current and the drain-source saturation voltage:

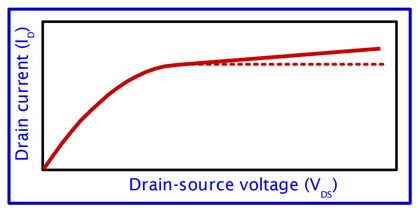
$$I_D = B(V_{GS} - V_{TH})^2 \Rightarrow I_D = B(V_{GS} - V_{TH})^{\alpha}$$

$$V'_{DO} = V_{GS} - V_{TH} \Rightarrow V'_{DO} = V_{DO}\left(\frac{V_{GS} - V_{TH}}{V_{DD} - V_{TH}}\right)^{\frac{\alpha}{2}}$$

4. CHANNEL LENGTH MODULATION AND DIBL EFFECTS

Channel length modulation (CLM) refers to the shortening of the length of the inverted channel region with increase in drain bias.

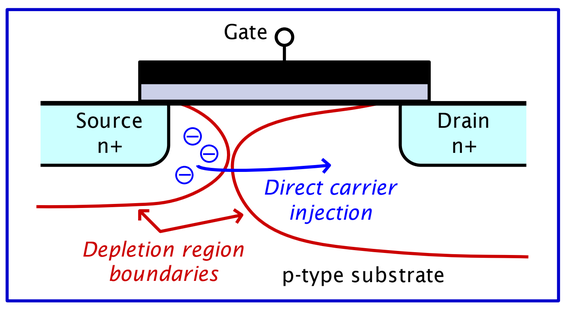




When the device operates in saturation and the drain voltage increases, the uninverted region at the vicinity of the drain (pinch-off region) expands toward the source, shortening the length of the channel region. Due to the fact that resistance is proportional to length, shortening the channel decreases its resistance, causing an increase in current with increase in drain bias for a device operating in saturation.

The effect is more pronounced when the source-to-drain separation is short (i.e. in deep-submicrometer and nanometer devices).

In a MOSFET device, a potential barrier exists between source and channel, which is controlled by the gate voltage. When the gate voltage is increased the barrier between the source and the channel is decreased, increasing the carriers injection from the source to the channel over the lowered barrier.



In very short-channel devices, as drain voltage increases, more depletion is performed by the drain bias, and the electric field at the drain penetrates to the source region caused an additional decrease of the barrier at source. This is referred as Drain Induced Barrier Lowering (DIBL) effect. As a result, the device can conduct significant drain current due to an increase of carriers injected from the source.

DIBL affects the drain current vs drain bias curve, causing the current to increase with drain bias in the saturation region of operation (i.e. at high drain-to-source voltages). This current increase is additional to that caused by the CLM effect.

The dependence between the drain current and the drain-source voltage in saturation region, which is due to CLM and DIBL effects, is modeled through the inclusion of 2 parameters (A, D):

$$I_D = B(V_{GS} - V_{TH})^{\alpha} \Rightarrow I_D = B(V_{GS} - V_{TH})^{\alpha}[A + D(V_{DS} - V_{DO})]$$

Given the practical target of the model, this linear dependence maintains the simplicity, while provides the required accuracy by including the influence of both effects.

5. BODY EFFECT

When a positive V_{SB} is applied, the bulk is at a negative potential with respect to the source, and this increases the depletion between the source and the bulk. The minority electrons attracted from the p-type bulk have to overcome this increase in depletion, and therefore the gate voltage required to form and maintain an inversion layer or channel (i.e. threshold voltage) becomes higher.

For the determination of the device threshold voltage when V_{SB} is positive, a linear approximation of the BSIM4 model expression describing the body effect is used:

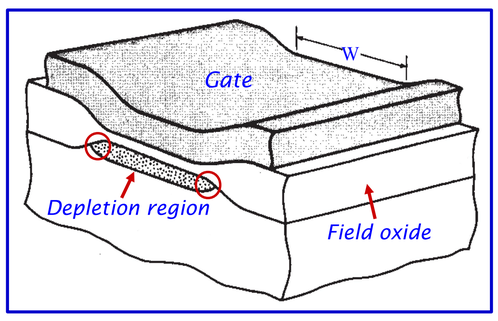
$$V_{TH} = V_{TO} + K_1(\sqrt{\varphi_s + V_{SB}} - \sqrt{\varphi_s}) + K_2 V_{SB} \Rightarrow V_{TH} = V_{TO} + \gamma V_{SB}$$

V_{TO}: threshold voltage for $V_{SB} = 0$, φ_s: inversion surface potential, K_1, K_2: BSIM4 body effect coefficients, γ: simplified body effect coefficient.

6. NARROW WIDTH EFFECT

In MOSFET devices, the depletion region is not limited to just the area below the thin oxide, since the polysilicon gate overlaps the field oxide on both sides of the channel region (along the width direction of the device). For large device widths the part of the depletion region on the sides is a small percentage of the total depletion region.

As the device width is scaled down, the depletion charge under the gate is reduced but the fringing charge remains relatively unchanged, constituting a significant proportion. The gate is responsible for depleting a larger region, so higher gate voltage is required, resulting in increased threshold voltage.



6. NARROW WIDTH EFFECT (cont'd)

In effect, this results in lower driving capability per width unit of narrow width devices in comparison with the driving capability per width unit of wide width devices.

The prediction of the drain current for varying device widths (i.e. the inclusion of narrow channel width effects) is obtained by computing the transconductance parameter B of the device as a quadratic function of the device channel width:

$$B = \beta_1 + \beta_2 W + \beta_3 W^2$$

The beta coefficients are determined by fitting the quadratic plot to the B vs W plot, respectively (once for a given technology).

7. SOURCE-DRAIN PARASITIC RESISTANCE

In long channel devices the source-drain resistance is negligible compared to the channel resistance. However, in very short-channel devices, becomes an appreciable fraction of the channel resistance and can cause significant current degradation.

The most severe current degradation occurs in the triode region, i.e. for low values of drain-source voltage. This is because the channel resistance is low (the slope of the drain current vs. drain-source voltage curve is high) under such bias conditions.

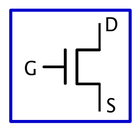
Since, the drain current dependence of the drain-source voltage is small in saturation, the current in this region is least affected by the parasitic resistance. The effect can be taken into account model by using lower transconductance parameter in the triode region than that in the saturation region.

8. PUTTING ALL TOGETHER

$$I_{Dtri} = B_{tri}(V_{GS} - V_{TH})^{\alpha}\left(2 - \frac{V_{DS}}{V'_{DO}}\right)\frac{V_{DS}}{V'_{DO}} \qquad V_{DS} \le V'_{DO}$$

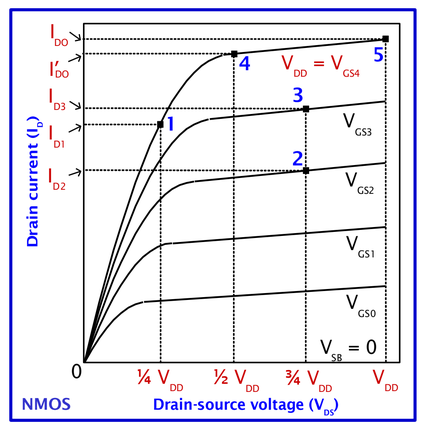
$$I_{Dsat} = B_{sat}(V_{GS} - V_{TH})^{\alpha}[A + D(V_{DS} - V_{DO})] \qquad V_{DS} > V'_{DO}$$

$$V'_{DO} = V_{DO}\left(\frac{V_{GS} - V_{TH}}{V_{DD} - V_{TH}}\right)^{\frac{\alpha}{2}} \qquad V_{TH} = V_{TO} + \gamma V_{SB}$$



$$B_{tri} = \frac{I'_{DO}}{(V_{DD} - V_{TH})^{\alpha}}, \quad B_{sat} = \frac{I_{DO}}{(V_{DD} - V_{TH})^{\alpha}}, \quad A = \frac{I'_{DO}}{I_{DO}}, \quad D = \frac{1 - A}{V_{DD} - V_{DO}}$$

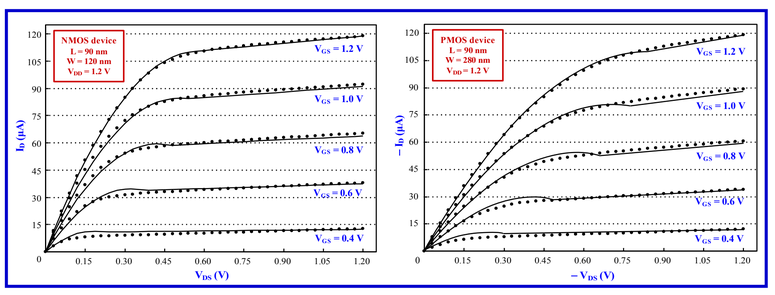
I_{DO}: drain current at $V_{GS} = V_{DS} = V_{DD}$, I'_{DO}: drain current at $V_{GS} = V_{DD}$ and $V_{DS} = 1/2 \cdot V_{DD}$ (for the NMOS device), $V_{DS} = 2/3 \cdot V_{DD}$ (for the PMOS device). By simulating the device, we obtain I_{DO} and I'_{DO} and consequently B_{tri} and B_{sat} for the minimum and the maximum used device width, as well as for few intermediate width values, in order to fit B vs W plots to quadratic plots.

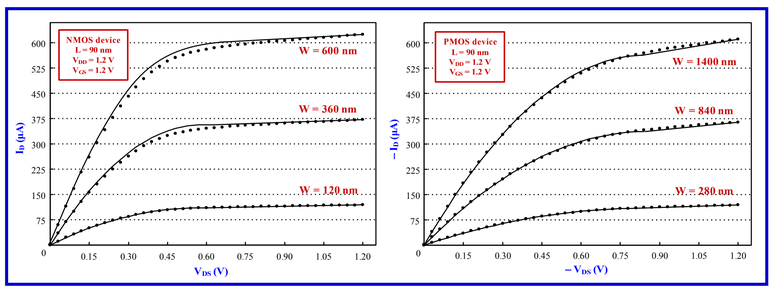


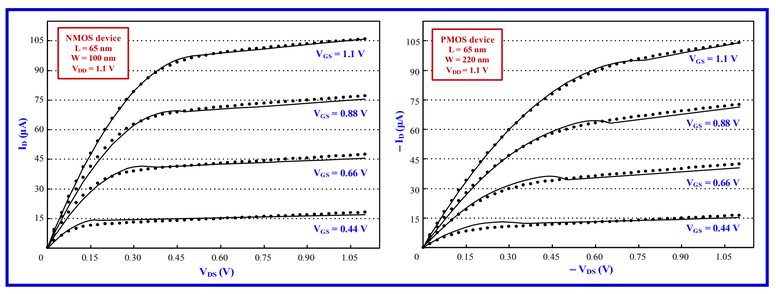
Velocity saturation index is extracted from I_{Dsat} expression by using the fitting points 2 and 3. V_{DO} is computed by combining I_{Dtri} and V'_{DO} expressions and using the fitting point 1:

$$\alpha = \frac{\ln\left(\frac{I_{D3}}{I_{D2}}\right)}{\ln\left(\frac{V_{GS3} - V_{TO}}{V_{GS2} - V_{TO}}\right)} \qquad V_{DO} = \frac{I'_{DO} V_{DD} + V_{DD}\sqrt{I'_{DO}(I'_{DO} - I_{D1})}}{4 I_{D1}}$$

9. EXPERIMENTAL RESULTS







Short-circuit energy dissipation model for sub-100nm CMOS circuits

1. INTRODUCTION

A considerable part of the energy dissipation in CMOS circuits is due to short-circuit currents. In this work, an accurate, analytical and compact model for this part of energy, i.e. the short-circuit energy dissipation, is presented. The model is based on closed-form expressions of the CMOS inverter output waveform, which include the influences of both transistor currents and the gate-drain coupling capacitance. An accurate version of the alpha-power law MOSFET model is used to relate the terminal voltages to the drain current in sub-100nm devices, with an extension for varying transistor widths. The resulting energy model accounts for the influences of input voltage transition time, transistors' sizes, device carrier velocity saturation and narrow-width effects, gate-drain and short-circuiting transistor's gate-source capacitances & output load.

2. MOSFET MODEL

For the expressions of the transistors' drain current, the following accurate and simple version of the alpha-power law MOSFET model is used.

$$I_D = B(V_{GS}-V_T)^{\alpha} \quad \text{for } V_{DS} > V'_{DO}$$

$$I_D = B(V_{GS}-V_T)^{\alpha}\left(2-\frac{V_{DS}}{V'_{DO}}\right)\frac{V_{DS}}{V'_{DO}} \quad \text{for } V_{DS} \le V'_{DO}$$

$$V'_{DO} = K(V_{GS}-V_T)^{\frac{\alpha}{2}} \qquad K = V_{DO}/(V_{DD}-V_T)^{\frac{\alpha}{2}}$$

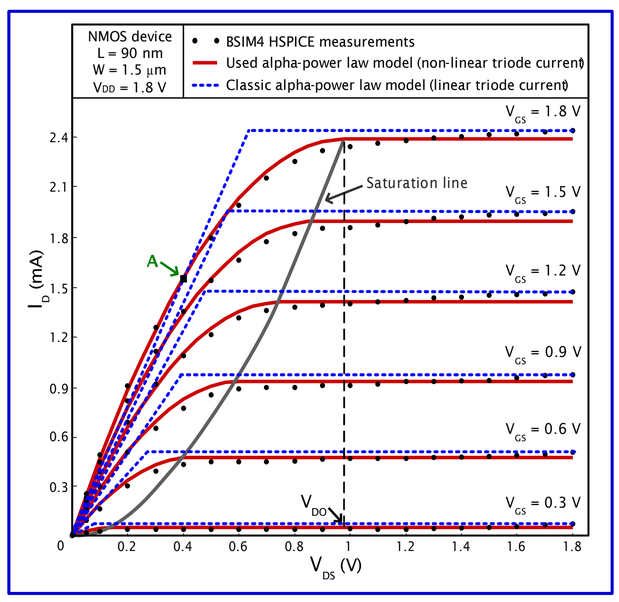
$$V_{DO} = \frac{BV_{DSA}(V_{DD}-V_T)^{\alpha}}{I_{DSA}} + \frac{\sqrt{BV_{DSA}^2(V_{DD}-V_T)^{\alpha}\,[B(V_{DD}-V_T)^{\alpha}-I_{DSA}]}}{I_{DSA}}$$

- V_{DD}: supply voltage
- V'_{DO}: drain-source saturation voltage
- V_T: threshold voltage
- α: velocity saturation index
- V_{DO}: drain-source saturation voltage at $V_{GS} = V_{DD}$
- B: transconductance parameter

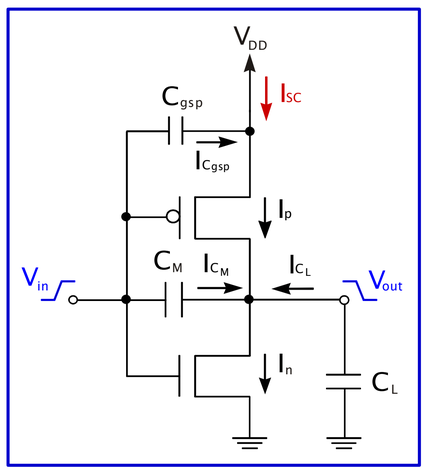
The last three model parameters are extracted from the MOSFET device output characteristics. To extend the model for higher device channel widths (W), the following equation is used:

$$B = \beta_1 + \beta_2 W + \beta_3 W^2$$

The coefficients β_i are determined by fitting a quadratic plot to the 'B vs W' plot (once for a given technology). The used MOSFET model is more accurate for sub-100 nm devices than the classic alpha-power model that uses linear drain current at the triode region (see figure below).



3. CMOS INVERTER



4. OUTPUT VOLTAGE WAVEFORM ANALYSIS

The output voltage waveform of the CMOS inverter is obtained for a rising input ramp: $V_{in} = V_{DD} \cdot (t/\tau)$ for $0 \le t \le \tau$, $V_{in} = 0$ for $t \le 0$ and $V_{in} = V_{DD}$ for $t \ge \tau$, where τ is the input voltage rise time. The analysis for a falling input is symmetrical.

The differential equation which describes the discharge of the load capacitance C_L for a CMOS inverter, taking into account the current through the gate-drain coupling capacitance (C_M) is written as:

4. OUTPUT VOLTAGE WAVEFORM ANALYSIS (cont'd)

$$C_L\frac{dV_{out}}{dt} = C_M\left(\frac{dV_{in}}{dt}-\frac{dV_{out}}{dt}\right)+I_p-I_n$$

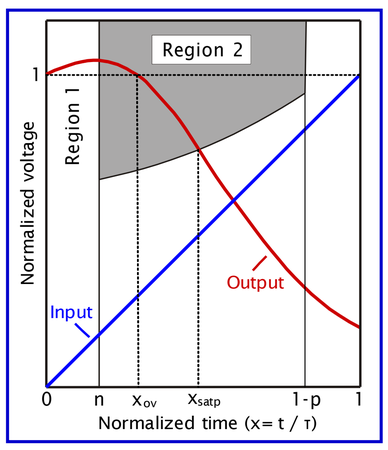
The gate-drain capacitance (C_M) is the sum of the gate-drain capacitances of both transistors, which consist of the gate-to-drain overlap capacitance and a part of the gate-to-channel capacitance. It is calculated by using C_{ox} (gate-oxide capacitance per unit area) and C_{gdo} (gate-drain overlap capacitance per unit channel width).

After normalizing voltages with respect to V_{DD} and using the variable $x = t/\tau$, the PMOS device current becomes:

$$I_p = \begin{cases} k_{lp1}(1-x-p)^{\alpha_p/2}(1-u_{out}) \\ \quad -k_{lp2}(1-u_{out})^2, & 1-u_{out} < u'_{dop} \\ k_{sp}(1-x-p)^{\alpha_p}, & 1-u_{out} \ge u'_{dop} \end{cases}$$

$$u'_{dop} = k_{vp}(1-x-p)^{\alpha_p/2}$$

k_{lpi}, k_{sp}, k_{vp} are constants depended on K_p, B_p, V_{DD}, α_p. The NMOS device current is given in a similar way.



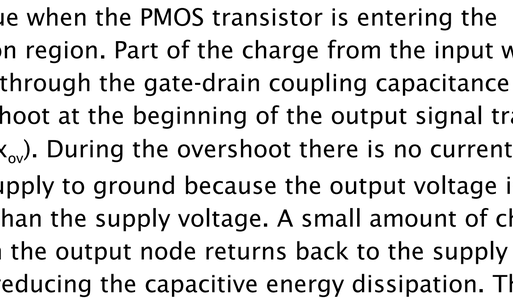
In region 1 ($0 \le x \le n$) the NMOS transistor is off and the PMOS transistor is in the linear region, while in region 2 ($n \le x \le x_{satp}$) the NMOS transistor is saturated and the PMOS transistor is still in the linear region. x_{satp} is the normalized time value when the PMOS transistor is entering the saturation region. Part of the charge from the input which injected through the gate-drain coupling capacitance causes an overshoot at the beginning of the output signal transition ($0 \le x \le x_{ov}$). During the overshoot there is no current from power supply to ground because the output voltage is greater than the supply voltage. A small amount of charge stored in the output node returns back to the supply node, slightly reducing the capacitive energy dissipation. The charge injected through C_M causes the main influence on the output signal in region 1. Since, the output node differential equation cannot be solved analytically, an average value of x (n / 2) is used in the first term of PMOS current, and an approximated expression for u_{out} ($1 + c_m x$, that is the output signal if only the charge through C_M is considered) in the quadratic term of the PMOS current.

$$u_{out} = 1+\frac{c_m}{C^3A_{lp1}^3}\left[2A_{lp2}c_m(e^{-xCA_{lp1}}-1)+2CA_{lp1}A_{lp2}c_m x + C^2A_{lp1}^2(1-e^{-xCA_{lp1}}-A_{lp2}c_m x^2)\right]$$

$$A_{lpi} = \frac{\tau\, k_{lpi}}{V_{DD}(C_L+C_M)} \qquad C = \left(1-p-\frac{n}{2}\right)^{\frac{\alpha_p}{2}} \qquad c_m = \frac{C_M}{C_L+C_M}$$

$$I_p = I_{p(n)} + S_1(x-n) \qquad I_{p(n)} = k_{lp1}(1-n-p)^{\alpha_p/2}(1-u_n)$$

In region 2, the PMOS current is approximated by a linear function of x:



The current slope S_1 is computed by equating the exact PMOS current in the linear region with the approximated one, at $x = (1-p)/2$. After that, the output voltage waveform in region 2, is described by:

$$u_{out} = u_n + c_m(x-n) + I_{p(n)}\,d(x-n) + \frac{S_1\,d(x-n)^2}{2} - \frac{A_{sn}(x-n)^{\alpha_n+1}}{\alpha_n+1} \qquad A_{sn} = \frac{k_{sn}\tau}{V_{DD}(C_L+C_M)} \qquad d = \frac{\tau}{V_{DD}(C_L+C_M)}$$

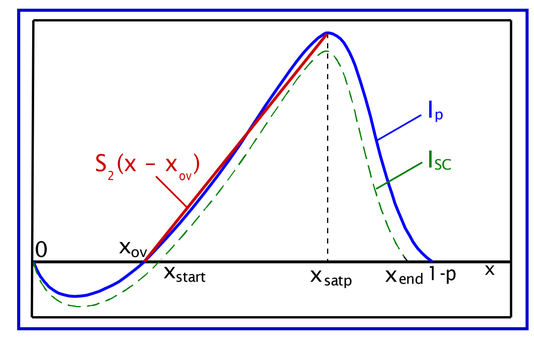
5. SHORT-CIRCUIT ENERGY DISSIPATION

The short-circuit energy dissipation for a rising input is the energy of the current (I_{SC}) which provided from the power supply. The current through the PMOS device includes two non-short-circuit current components: the current flowing through C_{gsp} and the current flowing from the output to the supply node during the overshoot of the output signal. Both current components are provided from the input and are independent of the load. The short-circuit energy dissipation during a falling output transition is defined as:

5. SHORT-CIRCUIT ENERGY DISSIPATION (cont'd)

$$E_{SC} = V_{DD}\int_{x_{start}}^{x_{end}} I_{SC}\,\tau\,dx = V_{DD}\left(\int_{x_{start}}^{x_{satp}} I_{SC}\,\tau\,dx + \int_{x_{satp}}^{x_{end}} I_{SC}\,\tau\,dx\right) \qquad I_{SC} = I_p - I_{C_{gsp}} \qquad I_{C_{gsp}} = C_{gsp}\left(\frac{V_{DD}}{\tau}\right)$$

A linear approximation of the PMOS transistor current is used in the first integral (as shown in the figure below), while in the second integral the PMOS saturation current is substituted. S_2 is the slope of I_p and is calculated by equating the exact PMOS current in the linear region with the approximated one, at the middle of the interval [x_{ov}, x_{satp}]. Both x_{ov}, x_{satp} are computed by using second order Taylor series expansions of u_{out} and u'_{dop}.



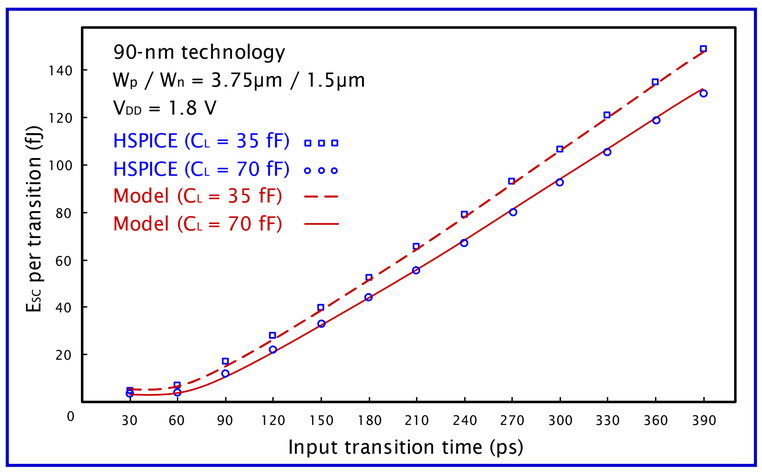
$$E_{SC} = \frac{V_{DD}}{2}(x_{satp}-x_{start})[(x_{satp}+x_{start}-2x_{ov})S_2 - \frac{2C_{gsp}V_{DD}}{\tau}] + \frac{V_{DD}k_{sp}\tau}{\alpha_p+1}[(1-p-x_{satp})^{\alpha_p+1} - (1-p-x_{end})^{\alpha_p+1}] - C_{gsp}V_{DD}^2(x_{end}-x_{satp})$$

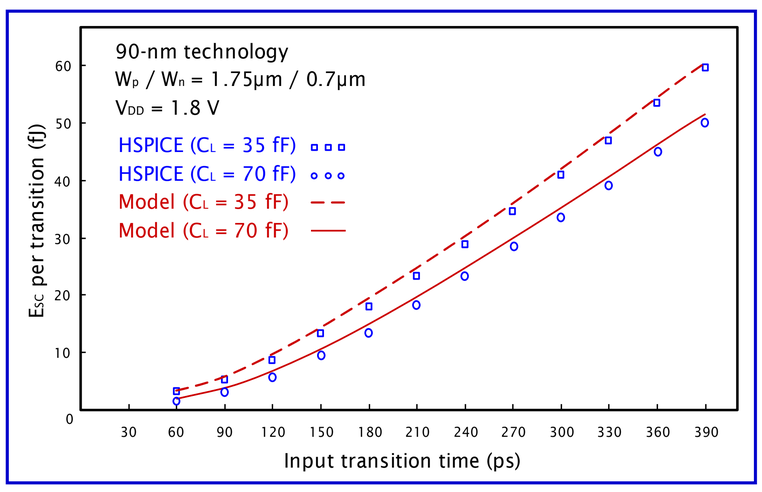
x_{start} is calculated by: $S_2(x_{start}-x_{ov}) - C_{gsp}(V_{DD}/\tau) = 0$

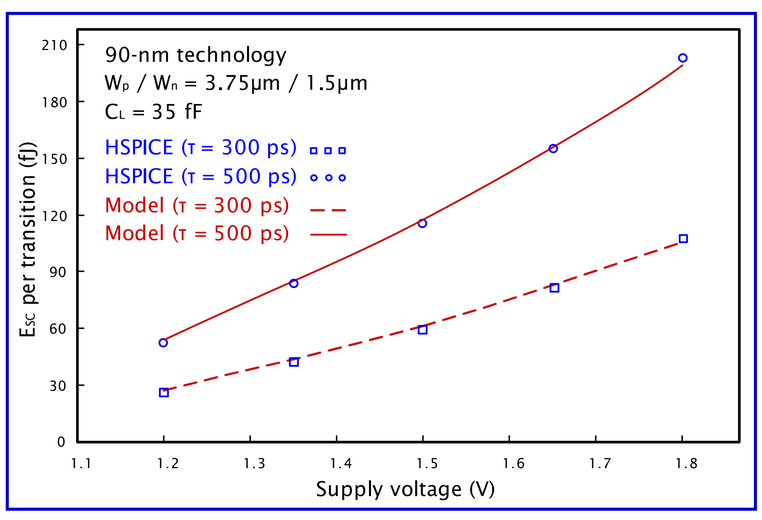
x_{end} is calculated by: $k_{sp}(1-x_{end}-p)^{\alpha_p} - C_{gsp}(V_{DD}/\tau) = 0$

6. EXPERIMENTAL RESULTS

The model has been validated for a 90-nm CMOS technology (PTM). In the first couple of figures below, the short-circuit energy per transition is plotted for different input transition times, capacitive loads and inverter sizes. The results show very good agreement with BSIM4 HSPICE simulations (average error is 3.5%). In addition, in the third figure, the short-circuit energy per transition is plotted as a function of the supply voltage, validating the accuracy of the model for the range of supply voltages applied in modern CMOS circuits. The derived model accounts for the influences of input voltage transition time, transistors' sizes, device carrier velocity saturation and narrow-width effects, gate-drain and short-circuiting transistor's gate-source capacitances, output load, and provides an analytical and accurate method for the evaluation of the short-circuit energy dissipation in sub-100nm CMOS buffers.



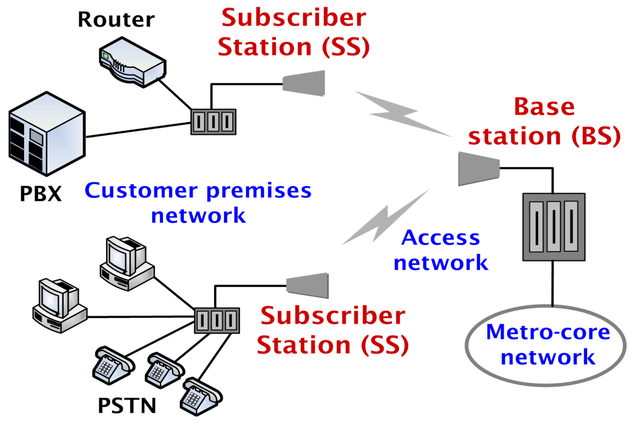




Efficient baseband model physical implementation for fixed broadband wireless access networks

1. INTRODUCTION

This poster presents the physical implementation of the digital part of an **OFDM-based baseband modem** for point-to-multipoint **fixed broadband wireless access (FBWA)** solutions. It is compliant with the **IEEE 802.16d standard** and compatible to a fixed WiMAX profile. The adopted realization approach is based on an array of processing elements belonging to a case of computing systems characterized by having hundreds of embedded processing elements and memories (massively parallel processor arrays, MPPAs). The approach offers the performance, the computational density and the programmability needed for the implementation of modern **wireless communication systems**.



Fixed wireless broadband is an alternative to DSL, providing services similar to those of traditional fixed-line broadband but using wireless as transmission medium. Fixed broadband wireless access (FBWA) solutions are usually being specified for point-to-multipoint applications, i.e. for use by residential customers and small to medium sized enterprises. They support a wide range of voice/data services, using a wireless system to connect the customer premises to other users & networks.

WiMAX (worldwide interoperability for microwave access) industry forum certifies broadband wireless solutions mainly based on the wireless metropolitan area networking (WMAN) standard developed by IEEE 802.16 group. In 2004, this group has completed and approved the IEEE 802.16d version of the standard, targeted fixed applications (usually referred as fixed WiMAX). Next versions of the standard concern nomadic and mobile applications and referred as mobile WiMAX. IEEE 802.16d covers fixed non-line-of-sight (NLOS) applications in the 2GHz - 11GHz band, using an orthogonal frequency division multiplexing (OFDM) physical layer (i.e. baseband modem). For practical reasons of interoperability, fixed WiMAX uses subsets of the standard's options (certification profiles), including 3.5GHz and 5.8GHz systems operating over 3.5MHz up to 10MHz channel and based on a 256-points FFT OFDM physical layer with a point-to-multipoint or mesh MAC layer. The profiles use frequency division duplexing (FDD) or time division duplexing (TDD).

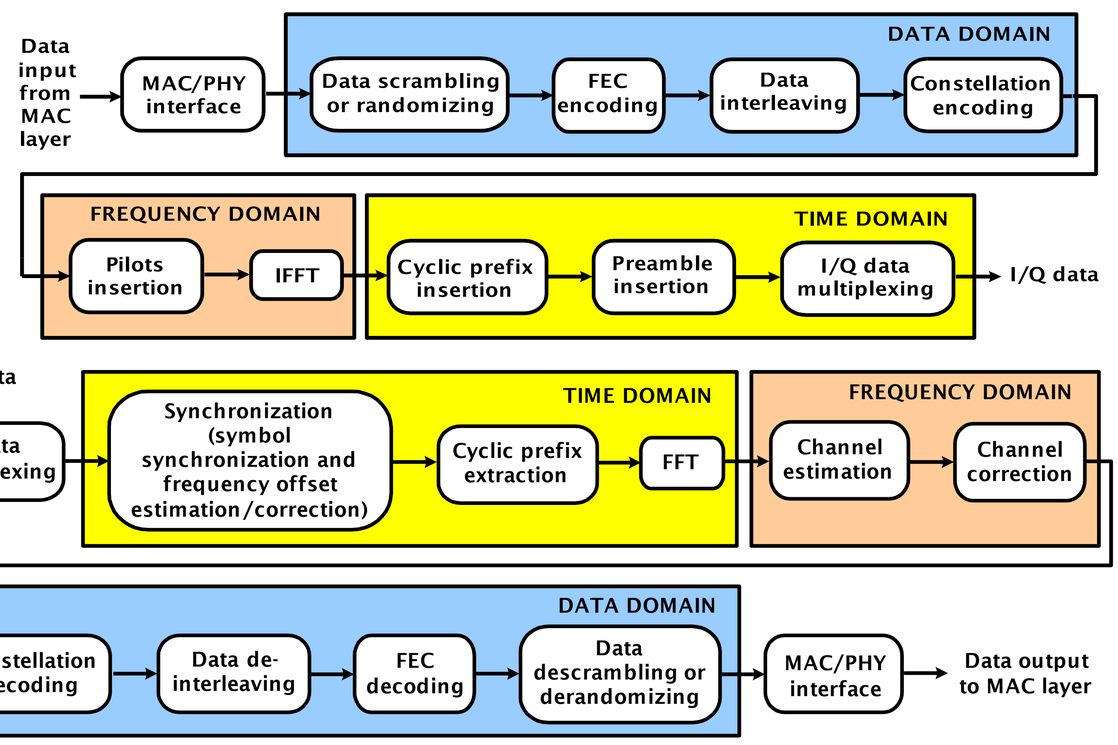
The realized OFDM-based physical layer is based on a 256-points FFT, uses TDD and operates over 10 MHz channel bandwidth, however it is parametric supporting 5 MHz. The adopted implementation approach is based on a **massively parallel processor array (MPPA)**. Traditionally, designers had to choose between rapid time-to-market with microprocessors, DSPs and FPGAs, and tight size, high-performance and low-power consumption using ASICs. MMPAs help to bridge this gap by offering programmability coupled with the ability to increase the computational density, accelerate the performance and reduce the power consumption of the designed system. The baseband modem is realized by using the picoArray architecture, containing several hundreds of heterogeneous processing elements, connected through a compile-time scheduled interconnect. The picoArray devices are designed to be connected together for multi-chip solutions and easily implement DSP applications, which require additional processing. The devices are supported by a complete tool suite in order to implement, debug and verify systems on them.

2. BASEBAND MODEM DESCRIPTION

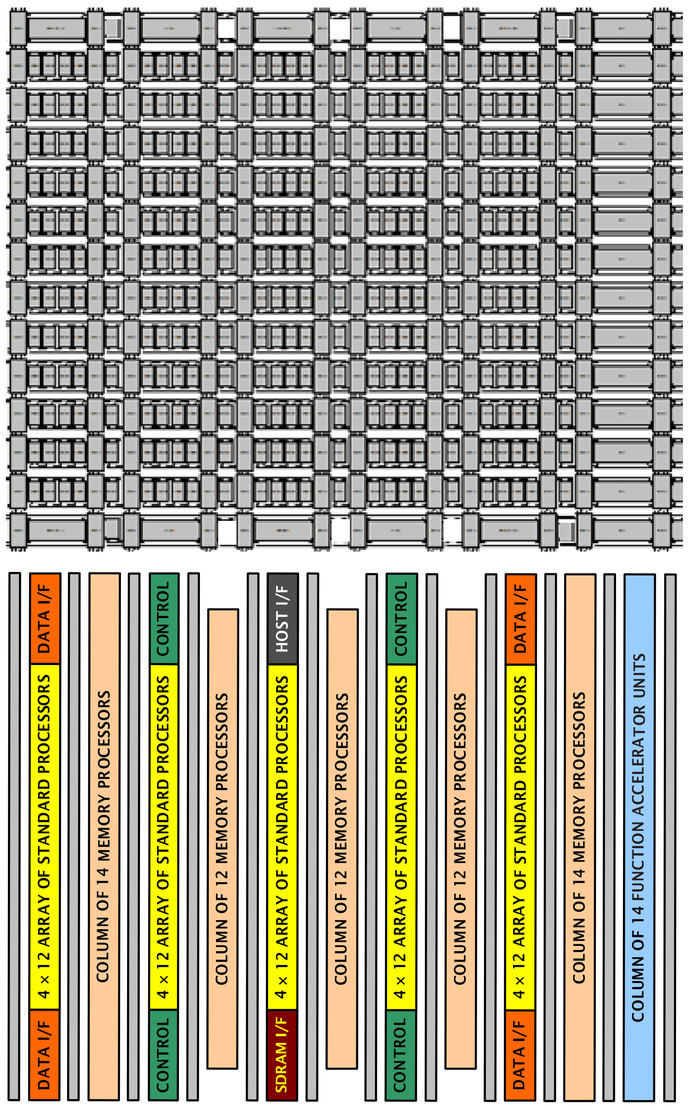
In the **transmit path** of the modem, initially the binary input data are randomized to prevent a long sequence of 1s and 0s, which will cause timing recovery problem at the receiver. The randomized data are fed to the Reed Solomon (RS) encoder, which is a part of forward error correction (FEC) encoder. The input data is over-sampled and parity symbols are calculated and appended with original data. Redundant bits are added to the actual message providing immunity against severe channel conditions. The error coded bits are further coded by convolutional encoder with a coding rate of ½ and a constraint length of 7. Since six different data rates are supported, proper puncture is applied after the convolutional encoding. The encoded data is passed through a bit interleaver; the bit interleaver size is set to the size of one OFDM symbol and the size of the symbol depends on the used modulation. The bits of a symbol are rearranged in a fashion so that adjacent bits to be placed on non-adjacent subcarriers. Interleaving is performed to protect the data from burst errors during transmission. The constellation encoder maps the input bits onto different subcarriers. Different modulation schemes are supported (BPSK, QPSK, 16-QAM and 64-QAM). The interleaved bits are divided in groups of 1, 2, 4 or 6 bits (data subcarriers) and mapped into complex numbers representing BPSK, QPSK, 16-QAM, 64-QAM values, respectively. The basic unit in data transmission is the OFDM symbol that consists of 192 data subcarriers. To facilitate channel estimation at the receiver, 8 pilot subcarriers are added to each 192 data subcarriers and by applying 256-points IFFT, the output is transformed into a time-domain signal. To make the transmit system robust to multipath propagation, a cyclic prefix (CP) is added to each OFDM symbol. The CP duration depends on the channel bandwidth (3–25% of the symbol duration). For a 10MHz spectrum, the symbol duration is 22.2μs and the adopted CP duration is 2.8μs (12.5%), leading in a total duration of 25μs.

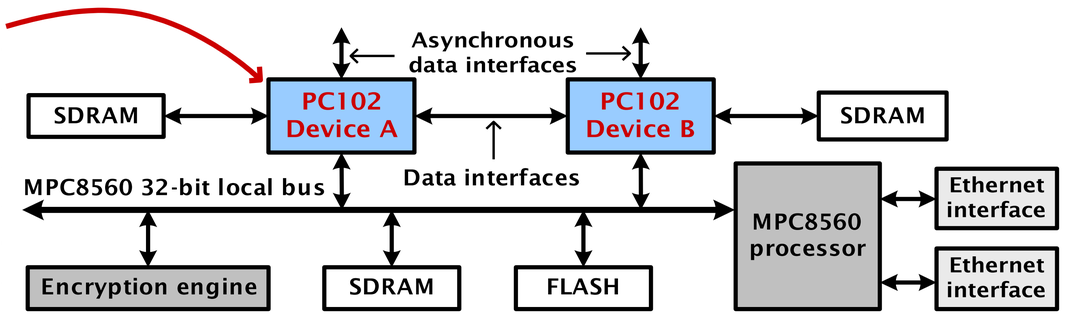
The symbols are packed into frames before sending. The adopted frame duration is 5ms. In the case of TDD, where the uplink and downlink transmissions occur at different (complementary) times while sharing the same frequency, each frame consists of the downlink and the uplink subframes. In each subframe proper preambles are inserted. The preambles are structured as either one of two symbols and transmitted before the data symbols to facilitate the synchronization tasks at the receiver. After the preambles, for each subframe, a frame control header of one symbol is transmitted. The last action of the transmit path is the multiplexing of the produced I/Q data, in order the digital output signals to be converted to the transmitted analog signal.

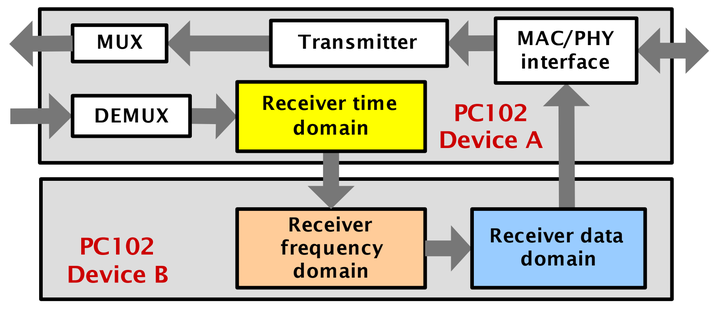
In the **receive path** after the demultiplexing of the I/Q data, and before the receiver can demodulate the subcarriers, it has to perform the synchronization tasks. Achieving synchronization involves detecting the symbol boundaries (to avoid inter-symbol interference) and estimating/correcting any frequency offsets in the received signal. Timing and frequency synchronization is achieved by utilizing the repetitive nature of the preambles. The time domain of the receiver is continued with the CP extraction and the transition of the received signal from the time to the frequency domain is achieved by applying a 256-points FFT. During reception, in order to recover the original signal at the receiver, the transfer function of the channel has to be estimated. Channel estimation is carried out by exploiting known data (pilot subcarriers), which are scattered at predefined locations inside OFDM symbols during transmission. The principle is to estimate the channel transfer function at pilot locations and then to achieve estimation for all data locations by performing a two-dimensional interpolation. Once the Channel estimates in each subcarrier position are obtained, channel correction has to be carried out. This task is performed by a frequency domain equalizer that is an array of complex multipliers (one for each subcarrier). In the data domain of the receive path, initially the decoding methods for the four modulation schemes are applied by the constellation decoder. Then, the data are deinterleaved and inserted to the FEC decoder that is a soft decision Viterbi decoder followed by an RS decoder, which recovers the original data. Finally, the decoded data are derandomized by using the same structure with that used at the transmitter.



3. PHYSICAL IMPLEMENTATION AND VALIDATION







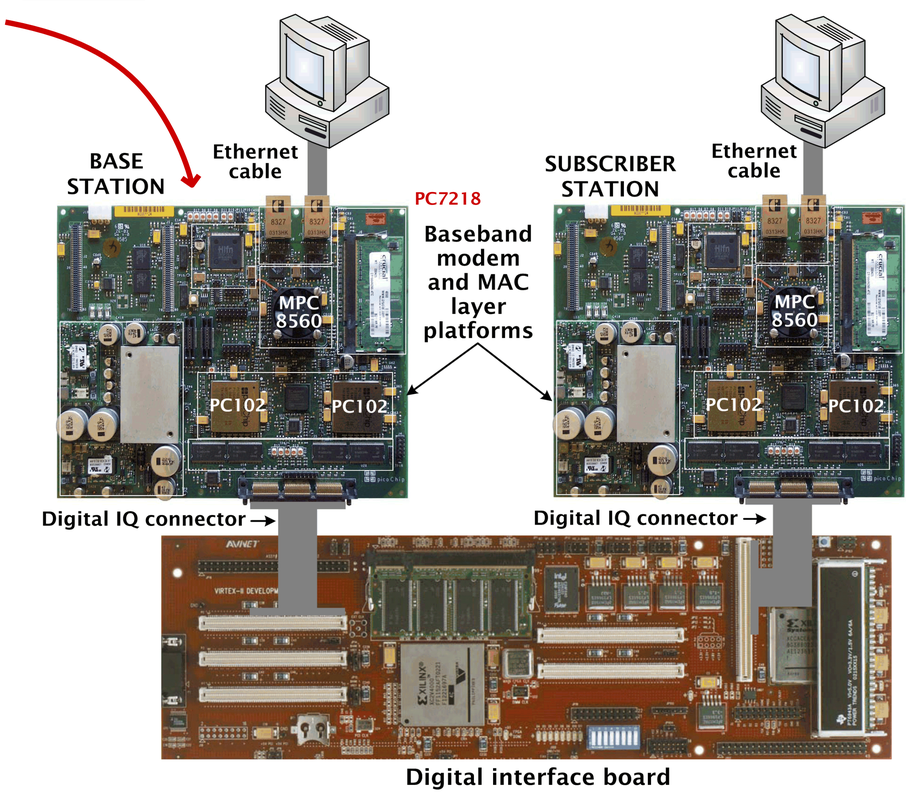
picoArray MPPA (PC102 device): Array with 322 processors that communicate over a network of 32-bit unidirectional buses and programmable bus switches.

16-bit RISC processors: 240 standard processors with 768 bytes memory and multiply-accumulate unit, 64 memory processors with 8704 bytes memory and multiply unit, 4 control processors with multiply unit and 65535 bytes memory. In addition, 14 function acceleration units with configurable hardware for accelerating computational intensive tasks.

Interfaces: Host interface, SDRAM interface, 4 data interfaces.

PC7218 hardware platform: 2 PC102 devices, MPC8560 processor (PowerPC core), encryption engine, Ethernet & digital I/Q interfaces, memory modules.

Tool chain: The algorithmic entities were described in C. Structural VHDL was used to describe the structure of the system including the relationship between entities and the connection signals. The input code is converted into a form suitable for execution on the MPPA by using a C compiler and a VHDL parser. The parser coordinates the compilation of the code and creates an internal representation for each entity and its signals. Whenever a block of C code is encountered the C compiler is invoked. A design browser, allows the design to be viewed graphically and a cycle accurate simulator allows the verification of the design before moving to hardware. After the mapping of entities to the MPPAs, the partitioning tool was used to handle the off-chip communication by using a pair of the data interfaces. The last steps were the final assignment of the devices to each entity, along with the routing of all the signals linking the entities, as well as the debugging of the design on the hardware.



Digital interface board

An elementary MAC layer version running at the host processor and providing a bridge for the data packets between the Ethernet interface and the digital transceivers. A digital interface of the two stations was realized in an FPGA device, hosted in a development board that ensures access to the inputs and the outputs of the device. Since, the channel bandwidth was set to 10MHz, operating using TDD scheme with a 3:1 downlink-to-uplink ratio, the peak data rate for 64-QAM modulation is about 34.5Mbps and 8.5Mbps for the downlink and the uplink, respectively. The receive capability is reduced (to 8Mbps), mainly due to the Viterbi decoding.
Demonstrated applications: Ping – transmit and response times were about 10ms and 25ms for the downlink and the uplink, respectively. File transfer – according to the file size and the transfer time, the average data rate was about 7.5Mbps. Video streaming – during the streaming of a video by the base station that was watched at the subscriber station with a typical media player, a data rate between 1Mbps & 3Mbps was observed (video rate was lower than the data rate that can achieve the developed system). Connection setup duration – duration of 100 frames (0.5s).